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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	1	of	10

Complete if Known	
Application Number	10/716,561
Filing Date	November 20, 2003
First Named Inventor	Craig C. HANSEN, et al.
Group Art Unit	2183
Examiner Name	CHAN, EDDIE P
Attorney Docket Number	43876-151

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
E.C.	AA	US-4,852,098	07/25/1989	Brechard, et al.	
	AB	US-4,875,161	10/17/1989	Lahti, et al.	
	AC	US-4,949,294	08/14/1990	Wambergue, et al.	
	AD	US-4,953,073	08/28/1990	Moussouris, et al.	
	AE	US-4,959,779	09/25/1990	Weber, et al.	
	AF	US-5,081,698	01/14/1992	Kohn	
	AG	US-5,113,506	05/12/1992	Moussouris, et al.	
	AH	US-5,155,816	10/13/1992	Kohn	
	AI	US-5,161,247	11/03/1992	Murakami, et al.	
	AJ	US-5,179,651	01/12/1993	Taaffe, et al.	
	AK	US-5,231,646	07/27/1993	Heath, et al.	
	AL	US-5,233,690	08/03/1993	Sherlock, et al.	
	AM	US-5,241,636	08/31/1993	Kohn	
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	AP	US-5,515,520	05/07/1996	Hatta, et al.	
	AQ	US-5,533,185	07/02/1996	Lentz, et al.	
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E.C.	AS	US-5,600,814	02/04/1997	Gahan, et al.	

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Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where RelevantPassages or Relevant Figures Appear	T[6]
E.C.	AT	WO 93/11500				

Examiner Signature		Date Considered	3/3/06

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Sheet 2 of 10

Complete if Known	
Application Number	10/716,561
Filing Date	November 20, 2003
First Named Inventor	Craig C. HANSEN, et al.
Group Art Unit	2183
Examiner Name	CHAN, EDDIE P
Attorney Docket Number	43876-151

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
E.C.	AU	IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563)	
	AV	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529)	
	AW	Gerry Kane et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018576 –848)	
	AX	IBM, "The PowerPC Architecture: A Specification For A New Family of RISC Processors," 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994) (50006DOC019229 – 767)	
	AY	Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (50006DOC018849 – 19228)	
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	BA	i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn	
	BB	Gove, "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conference, pp. 215-24 (March 1994) (51056DOC000891 – 900)	
	BC	Gove, "The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," IEEE DSP Workshop, pp. 27-30 (October 2-5, 1994) (51056DOC015452 – 455)	
	BD	Guttag et al., "A Single-Chip Multiprocessor for Multimedia: The MVP," IEEE Computer Graphics & Applications, pp. 53-64 (November 1992) (51056DOC000913 – 924)	
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	BH	Bass et al., "The PA 7100LC Microprocessor: A Case Study of IC Design Decisions in a Competitive Environment," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 12-22 (April 1995) (51056DOC059283 – 289)	
	BI	Bowers et al., "Development of a Low-Cost, High Performance, Multiuser Business Server System," Hewlett-Packard Journal, Vol. 46, No. 2, p. 79 (April 1995) (51056DOC059277 – 282)	
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E.C.	BN	Lee et al., "Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7100LC Processors," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 60-68 (April 1995) (51056DOC013549 – 557)	

Examiner Signature	Eric Chan	Dated Considered	3/3/06

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Filing Date	November 20, 2003
First Named Inventor	Craig C. HANSEN, et al.
Group Art Unit	2183
Examiner Name	CHAN, EDDIE P
Attorney Docket Number	43876-151

U.S. PATENT DOCUMENTS

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EC	BO	US-5,636,351	06/03/1997	Lee	
	BP	US-5,721,892	02/24/1998	Peleg, et al.	
	BQ	US-5,734,874	03/31/1998	Van Hook, et al.	
	BR	US-5,758,176	05/26/1998	Agarwal, et al.	
	BS	US-5,768,546	06/16/1998	Kwon	
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	BU	US-5,996,057	11/30/1999	Scales III, et al.	
	BV	US-6,425,073	07/23/2002	Roussel, et al.	
EC	BW	US-6,516,406	02/04/2003	Peleg, et al.	

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Examiner Signature	Eric Chan	Date Considered	3/3/06

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/716,561
				Filing Date	November 20, 2003
				First Named Inventor	Craig C. HANSEN, et al.
(use as many sheets as necessary)				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	4	of	10	Attorney Docket Number	43876-151

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
EC	BX	Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 – 351)	
	BY	Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 – 090)	
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	CA	HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 – 141)	
	CB	PA-RISC 1.1 Architecture and Instruction Set Reference Manual, Third Edition, Hewlett-Packard (February 1994) (51056DOC002157 – 176)	
	CC	Ang, "StarT Next Generation: Integrating Global Caches and Dataflow Architecture," Proceedings of the ISCA 1992 Dataflow Workshop (1992) (51056DOC071743 - 776)	
	CD	Beckerle, "Overview of the StarT (*T) Multithreaded Computer," IEEE COMPCON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 – 519)	
	CE	Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 – 751)	
	CF	Gipper, "Designing Systems for Flexibility, Functionality, and Performance with the 88110 Symmetric Superscalar Microprocessor," IEEE (1992) (51056DOC008758 – 763)	
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	CM	J. Arends, "88110: Memory System and Bus Interface," Northcon, 1992 (51056DOC009739 – 742)	
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	CO	J. Maguire, "MC88110: Datpath," Northcon, 1992 (51056DOC010059 – 063)	
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	CQ	Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 – 661)	
	CR	Knapp et al., "Bulk Storage Applications in the ILLIAC IV System," ILLIAC IV Document No. 250, Center for Advanced Computation, University of Illinois at Urbana-Champaign (August 3, 1971) (51056DOC001647 – 656)	
	CS	Awaga et al., "The μVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 – 934)	
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Examiner Signature	Eric Coleman	Dated Considered	3/3/06

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First Named Inventor	Craig C. HANSEN, et al.
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

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EC	CU	Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 – 194)	
	CV	Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 – 607)	
	CW	Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)	
	CX	Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 -034)	
	CY	Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 – 279)	
	CZ	Widdoes, "The S-1 Project: Developing High-Performance Digital Computers," IEEE Computer Society COMPCON Spring 1980 (December 11, 1979) (51056DOC071574 - 585)	
	DA	Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895)	
	DB	The S-1 Project, January 1985, S-1 Technical Staff (51056DOC057368 – 607)	
	DC	S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 – 918)	
	DD	Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758)	
	DE	Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618)	
	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)	
	DG	Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376)	
	DH	Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157)	
	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)	
	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)	
	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)	
	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)	
	DM	Saturn Overview (November 12, 1993) (51056DOC017111 - 157)	
	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 – 7510)	
	DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)	
	DP	Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 – 443)	
	DQ	Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 – 459)	
	DR	Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 – 5299)	
EC	DS	Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394)	

Examiner Signature	Eric Coleman	Dated Considered	3/3/06

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EC	DT	Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	
	DU	AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	
	DV	Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 – 666)	
	DW	Grimes et al., "A New Processor with 3-D Graphics Capabilities," NCGA '89 Conference Proceedings Vol. 1, pp. 275-84 (April 17-20, 1989) (5156DOC070711 – 717)	
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	DY	Kohn et al., "A 1,000,000 Transistor Microprocessor," 1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, 290 (February 15, 1989) (51056DOC072091 – 094)	
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	EB	Kohn et al., "The i860 64-Bit Supercomputing Microprocessor," AMC, pp. 450-56 (1989) (51056DOC000330 – 336)	
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	EJ	Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 – 9097)	
	EK	N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	
	EL	N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	
	EM	N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	
	EN	N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	
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EC	ER	Moussouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 – 630)	

Examiner Signature	Eric Coleman	Dated Considered	3/3/06

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	10/716,561
				Filing Date	November 20, 2003
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
(use as many sheets as necessary)				Examiner Name	CHAN, EDDIE P
Sheet	7	of	10	Attorney Docket Number	43876-151

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS); title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
EC	ES	Arnould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 – 958)	
	ET	Bell, "Ultracomputers: A Teraflop Before Its Time," Communications of the ACM, (August 1992) pp. 27-47 (51056DOC020903 – 923)	
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	FJ	Litzkow et al., "Condor – A Hunter of Idle Workstations," IEEE (1988) (51056DOC068712 – 719)	
	FK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 – 628)	
EC	FL	Nienhaus, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 – 471)	
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Examiner Signature	Eric Chan	Dated Considered	3/3/06

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 8 of 10

Complete if Known	
Application Number	10/716,561
Filing Date	November 20, 2003
First Named Inventor	Craig C. HANSEN, et al.
Group Art Unit	2183
Examiner Name	CHAN, EDDIE P
Attorney Docket Number	43876-151

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T[2]
EC	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 – 948)	
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 – 887)	
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110 118) (51056DOC002949 – 957)	
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	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)	
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 – 946)	
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	FU	Tolmie, "HIPPI: It's Not Just for Supercomputers Anymore," Data Communications (May 8, 1995) (51056DOC071802 - 809)	
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	FX	Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 – 256)	
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	GD	Data General AViiON AV500, 550, 4500 and 5500 Servers	
	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)	
	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)	
	GG	National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 – 243)	
EC	GH	Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757)	

Examiner Signature	Eric Chan	Dated Considered	3/3/06

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				Filing Date	November 20, 2003
				First Named Inventor	Craig C. HANSEN, et al.
(use as many sheets as necessary)				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	9	of	10	Attorney Docket Number	43876-151

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EC	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323)	
		Original Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004	
	GJ	Amended Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004	
	GK	Expert Witness Report of Richard A. Killworth, Esq., *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005	
	GM	Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005	
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005	
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005	
	GP	Request for *Inter Partes* Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005	
	GQ	Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GR	Deposition of Leslie Kohn on September 22, 2005; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division	
	GS	Intel Article, *"Intel Announces Record Revenue of 9.96 Billion"*, October 18, 2005	
	GT	The New York Times Article, *"Intel Posts 5% Profit Increase on Demand for Notebook Chips"*, October 19, 2005	
	GU	USA Today Article, *"Intel's Revenue Grew 18% In Robust Quarter for Tech"*, October 19, 2005	
	GV	The Wall Street Journal Article, *"Intel Says Chip Demand May Slow"*, October 19, 2005	
EC	GW	The New York Times Article, *"Intel Settlement Revives A Fading Chip Designer"*, October 20, 2005	

Examiner Signature	Eric Chan	Dated Considered	3/3/06

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)	ATTY. DOCKET NO. 043876-0151	SERIAL NO. 10/716,561
	APPLICANT Craig HANSEN, et al.	
	FILING DATE November 20, 2003	GROUP 2183

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC	A	US	6,643,765	11-04-2003	Hansen et al.	
EC	B	US	6,725,356	04-20-2004	Hansen et al.	
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
EC	C	MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005)	
EC	D	Intel Press Release, "Intel Announces Record Revenue of $9.96 Billion," Santa Clara, CA, 10-18-2005	

EXAMINER	DATE CONSIDERED
Eric Colan	3/3/06

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-151	**Continuati n f Applicati n No. 10/436,340**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **November 20, 2003**	GROUP: **To be assigned**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Doument Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EC		US	4,876,660	10/24/89	Owen et al.	
		US	4,956,801	09/11/90	Priem et al.	
		US	4,969,118	11/06/90	Montoye et al.	
		US	5,032,865	07/16/91	Schlunt	
		US	5,408,581	04/18/95	Suzuki et al.	
		US	5,500,811	03/19/96	Corry	
		US	5,557,724	9/17/1996	Sampat et al.	
		US	5,588,152	12/24/1996	Dapp et al.	
		US	5,640,543	6/17/1997	Farrell et al.	
		US	5,757,432	5/26/1998	Dulong et al.	
		US	5,802,336	9/1/1998	Peleg et al.	
		US	5,809,292	9/15/1998	Wilkinson et al.	
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EC		US	5,825,677	10/20/1998	Agarwal et al.	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number-Kind Codes (if known)	Publication Date MYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
EC		EP 0474246 A2	9/6/1991				
EC		EP 0654733 A1	7/5/1994				

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EC		L. Kohn et al. "The Visual Instruction Set (VIS) in UltraSPARC" IEEE. 1995. 462-469.	
		D. Shaver. "A General-Purpose Array Processor for Seismic Processing" (Nov - Dece 1984) January - March 1998. 15th Anniversary Issue. 5-26.	
		R. Lee. "Accelerating Multimedia with Enhanced Microprocessors" IEEE Micro. April 1995. 22-32.	
		N. Margulis. "i860 Microprocessor Architecture" 1990. 8-10, 171-175, 182-183.	
EC		A. Levinthal et al. "Parallel Computers for Graphics Applications" 1987. 193-198.	

EXAMINER	DATE CONSIDERED
Eric Cole	3/3/06

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(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-151	**Continuati n f Applicati n No. 10/436,340**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **November 20, 2003**	GROUP: **To be assigned**

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EC.		US	5,835,782	11/10/1998	Lin et al.	
		US	5,886,732	3/23/1999	Humpleman	
		US	5,922,066	7/13/1999	Cho et al.	
		US	5,983,257	11/9/1999	Dulong et al.	
		US	6,016,538	1/18/2000	Guttag et al.	
		US	6,092,094	7/18/2000	Ireton	
		US	6,401,194 B1	6/4/2002	Nguyen et al.	
		US	4,025,772	5/24/1977	Constant	
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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-151	Continuation of Application No. 10/436,340
APPLICANT: Craig HANSEN, et al.	
FILING DATE: November 20, 2003	GROUP: To be assigned

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
C.C.		US	5,201,056	4/6/1993	Daniel et al.	
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EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number-Kind Codes (if known)	Publication Date MYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No

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EXAMINER: Eric Cole

DATE CONSIDERED: 3/3/06

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(Suppl.)INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
43876-151	**C ntinuati n f Serial N . 10/436,340**
APPLICANT: **Craig HANSEN, et al.**	
FILING DATE: **November 20, 2003**	GROUP: **To be assigned**

U.S. PATENT DOCUMENTS

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
043876-0151	10/716,561
APPLICANT: HANSEN, C., et al.	
FILING DATE: November 20, 2003	GROUP: 2818

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	APPLICANT HANSEN, C., et al.	
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